

## **Report on the Seminar on Recent Trends in VLSI Design, Challenges and Opportunities**

A Seminar on “Recent Trends in VLSI Design Challenges and Opportunities” was organized by Department of Electronics and Communication Engineering, S.E.A College of Engineering and Technology, Bangalore on 15<sup>th</sup> October, 2022. The Seminar was conducted in AC Seminar Hall, S.E.A College of Engineering and Technology from 10.30 am to 12.30 pm. The seminar was arranged for final year and pre final year students. Nearly 50 students participated in the seminar. The function was presided by Dr.B.Venkatanarayana, Principal, SEACET and introduction of resource person was given by Dr. Pradeep Kumar N.S., HOD, ECE, SEACET.

### **About Seminar:**

The poster is for a seminar titled "Recent Trends in VLSI Design, Challenges and Opportunities". It is organized by S.E.A College of Engineering and Technology, Bangalore. The seminar is a one-day event held on 15<sup>th</sup> October 2022 at 10.30 AM in the AC Seminar Hall. The resource person is Mr. Prasad Rallabandi from IC Labs. The poster also mentions the association with IQAC and the Institution's Innovation Council. The background is blue with various logos and images related to VLSI design, including a microchip and a circuit diagram.

**S.E.A COLLEGE OF ENGINEERING AND TECHNOLOGY**  
KATA BAGAR, K.R.PURAM, BANGALORE-49

**A One day Seminar on**  
**"Recent Trends in VLSI Design, Challenges and Opportunities"**  
**In Association with IQAC and**  
**IC Labs**  
**On 15<sup>th</sup> October 2022 at 10.30 AM**

**Resource Person : Mr. Prasad Rallabandi**  
**IC Labs.**

**Venue: AC Seminar Hall**

### **Objective of the Seminar:**

The core objective of this Seminar is to enhance students to learn the concepts in VLSI Domain implementation and what are the challenges and opportunities in it. This Seminar will give the idea about basics of VLSI Design, Importance of the design engineer in VLSI, Development of IC's from the origin, and the role of IC design engineers in the core field. It will help to upgrade the expertise and capabilities of the students towards their academic excellence.

## Resource Person of the Seminar:

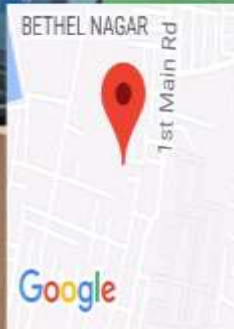
Resource Person of the seminar was Mr. Prasad Rallabandi, IC Labs Bangalore and Founder and Chief Executive Officer @ Thinsil Technologies. He is skilled in SystemVerilog, IC, VLSI, ASIC, Debugging, SoC, TCL, Verilog, RTL design and Static Timing Analysis

## Insights from Seminar:

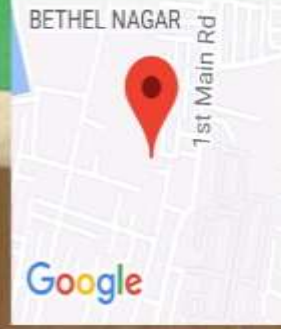
Mr. Prasad Rallabandi, IC Labs Bangalore delivered the topic in “Recent Trends in VLSI Design Challenges and Opportunities”. The digital hardware design flow was explained in detail. He briefed about timing analysis about digital circuits and the need for low power VLSI chips. He elaborated about challenges faced in IC design. He explained his vision to create highly skilled and enthusiastic VLSI Design engineers for the future semiconductor industry needs. How to equip students in Research Oriented Approach, Conceptual Learning and Gain theoretical knowledge along with its practical relevance. Research oriented teaching helps students involve deeper into concepts and enhance their learning competence and develop an appetite for critical thinking required for job. Later they explained about their company how they train students such that IC Labs IN is the solution to all your VLSI Design questions. To Start their career with skilled VLSI professionals, to make their career successful with diligence, enthusiasm, and dedication.

Snapshots from seminar are presented below.



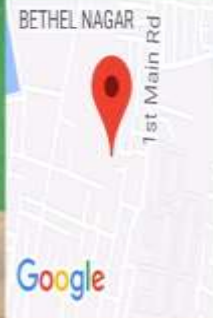


Bethel Nagar  
1st Main Rd  
Bengaluru Karnataka India 27°C  
17, 1st Main Rd, Bethel Nagar,  
Krishnarajapura, Bengaluru, Karnataka  
Lat: 13.01 | Long: 77.72  
15/10/2022 11:03 am, IST  
Sat, 15 Oct

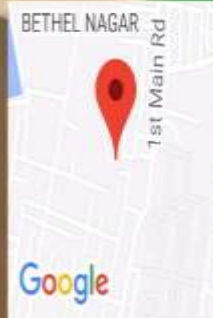


Bethel Nagar  
1st Main Rd  
Bengaluru Karnataka India 27°C  
17, 1st Main Rd, Bethel Nagar,  
Krishnarajapura, Bengaluru, Karnataka  
Lat: 13.01 | Long: 77.72  
15/10/2022 10:56 am, IST  
Sat, 15 Oct





BETHEL NAGAR  
Bengaluru Karnataka India 27°C  
17, 1st Main Rd, Bethel Nagar,  
Krishnarajapura, Bengaluru, Karnataka  
Lat: 13.01 | Long: 77.72  
15/10/2022 10:56 am, IST  
Sat, 15 Oct

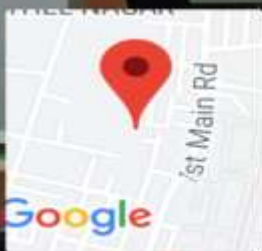


BETHEL NAGAR  
Bengaluru Karnataka India 27°C  
17, 1st Main Rd, Bethel Nagar,  
Krishnarajapura, Bengaluru, Karnataka  
Lat: 13.01 | Long: 77.72  
15/10/2022 10:56 am, IST  
Sat, 15 Oct



**Physical Design**

- Physical Design
  - Floor planning
  - Power planning
  - Placement
  - CPL
  - Routing
  - Clock (Setup, Hold, Jitter, Skew, Delay, Rise)
- Challenges:
  - Timing
  - Power
  - Signal Integrity
  - Trade



**Bengaluru, Karnataka, India**

17, 1st Main Rd, Bethel Nagar, Krishnarajapura, Bengaluru,  
Karnataka 560049, India

Lat 13.008554°

Long 77.716771°

15/10/22 11:59 AM GMT +05:30

GPS Map Camera



The Seminar was concluded at 12.30pm. The workshop ended with the vote of thanks by Dr. Pradeep Kumar N.S., HOD, ECE, SEACET. Feedback form was collected at the end of the seminar from the students. The Seminar was highly informative and thus provided valuable awareness and insights on the various aspects of in VLSI Design.